I. Final Rejection Improper

The outstanding Office Action states that the action was made final because the amendment made by Applicants necessitated the new ground(s) of rejection. In accordance with M.P.E.P. §706.07(a), Applicants respectfully assert that the final rejection in the outstanding Office Action was premature. Thus, Applicants respectfully request that the Examiner withdraw the finality of the rejection as a matter of record.

Under present practice, second or any subsequent action on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by Applicants' amendment of the claims nor based on information submitted in an information disclosure statement. M.P.E.P. §706.07(a). Therefore, a final rejection is premature where three conditions are met: (1) the Examiner introduces a new ground of rejection; (2) the new ground of rejection is not necessitated by Applicants' amendment of the claims; and (3) the new ground of rejection is not based on information submitted in the information disclosure statement. Applicants respectfully assert that the final rejection in the outstanding Office Action was premature.

Regarding the first condition, the outstanding Office Action does introduce a new grounds for rejection. More specifically, in the First Office Action mailed November 7, 2001, the Examiner indicated that "[c]laims 6 – 8 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. §112, second paragraph . . . " The Examiner further stated that "claims 6 – 8 would be allowable because the prior art of record fails to teach or fairly suggest" the claimed transistor circuit. In Applicants' "First Response and Amendment," claims 6 – 8 were amended to overcome the rejection under 35 U.S.C. §112, second paragraph by changing the word "third" to the word "second" in independent claim 6.

However, in the outstanding Office Action, the Examiner did not allow claims 6 – 8 as stated in the First Office Action. Rather, the outstanding Office Action now rejects claims 6 – 8 (which were previously indicated as having allowable subject matter) under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. No. 4,752,703 to Lin. Clearly, a rejection under 35 U.S.C. §102(b) where the claims were previously rejected under 35 U.S.C. §112, second paragraph and where the claims were previously regarded as having allowable subject matter if rewritten or amended to overcome the rejection under 35 U.S.C. §112, second paragraph is a new grounds of rejection,. Therefore, Applicants respectfully submit that the rejection of claims 6 – 8 in the outstanding Office Action under 35 U.S.C. §102(b) is a new grounds of rejection.

Regarding the second condition, Applicants respectfully assert that the new grounds of rejection under 35 U.S.C. §102(b) was *not* necessitated by Applicants' amendment of claims 6 – 8. As stated above, the amendment to claims 6 – 8 merely changed the word "third" to the word "second" in independent claim 6. This amendment did not add any new limitations to the claims. In fact, the amendment was made to comply with the Examiner's indication of allowable subject matter in the First Office Action. In response to Applicants' First Response and Amendment, instead of allowing claims 6 – 8, the Examiner performed an additional search to find the art cited in the new grounds of rejection under 35 U.S.C. §102(b) – U.S. Patent No. 4,752,703. Thus, Applicants' respectfully assert that the new grounds of rejection of claims 6 – 8 under the newly-cited art was not necessitated by the Applicants' amendments. The Examiner had every opportunity to search and locate U.S. Patent No. 4,752,703 in the initial search. However, the Examiner did not locate this reference, and instead indicated that claims 6 – 8 were allowable. Furthermore, the amendment to claims 6

– 8 did not add any new limitation and therefore did not necessitate the additional search and new grounds of rejection.

In fact, the M.P.E.P. is very clear that this type of action violates Applicants' due process. Specifically, "the Examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal." M.P.E.P. §706.07. In this regard, "[s]witching . . . from one set of references to another by the examiner in rejecting in successive actions claims of substantially the same subject matter, will alike tend to defeat attaining the goal of reaching a clearly defined issue for an early termination, i.e., either an allowance of the application or a final rejection." *Id.* As stated above, in the present case, the Examiner indicated that claims 6 – 8 contained allowable subject matter in the First Office Action. In the Second Office Action, the Examiner reneges on the allowable subject matter of claims 6 – 8 and then asserts a ***final*** rejection of the claims under 35 U.S.C. §102(b) as being anticipated by art that was not of record. Unlike the situations detailed in the M.P.E.P. in which final rejections are proper (*e.g.*, where an applicant switches from one claimed subject matter to another claimed subject matter in successive stages of prosecution), in the present case, Applicants have never switched the claimed subject matter. In fact, Applicants had no reason to switch the claimed subject matter because the First Office Action indicated that the claimed subject matter would be allowable. A failure to withdraw the premature final rejection in the instant case will deprive Applicants' of a full and fair hearing regarding claims 6 – 8. Accordingly, Applicants respectfully request that the Examiner withdraw the finality of the rejection as a matter of record.

Regarding the third condition, Applicants repeat that the new grounds of rejection under 35 U.S.C. §102(b) is based on art that was not submitted in an information disclosure

statement and which was not art of record. Specifically, U.S. Patent No. 4,752,703 was not listed in the Notice of References Cited in the First Office Action, but was included in the Notice of References cited in the Second Office Action after performing an additional search. Therefore, Applicants respectfully assert that the final rejection in the outstanding Office Action was in fact premature. Thus, Applicants respectfully request that the Examiner withdraw the finality of the rejection as a matter of record

II. Present Status of Patent Application

Upon entry of this response claims 1 – 8 are pending in the present application. Claims 1 - 5 have been amended as set forth above. Support for this amendment is found in the specification and in the original claims. No new matter has been added.

In addition to pointing out that the final rejection in the outstanding Office Action was premature and should therefore be withdrawn, Applicants address each of the outstanding objections and rejections in order to facilitate allowance of the pending claims and issuance of the present application.

III. Objection to Drawings

The Office Action objects to the drawings under 37 CFR 1.83(a). The Office Action argues that the drawings fail to show every feature of the invention specified in the claims. Specifically, the Office Action states that "the recitations 'a control signal' and 'the control signal' on lines 6 and 8 of claim 3 must be shown or the feature(s) canceled from the claim(s)."

Applicants respectfully disagree with the application of 37 CFR 1.83(a) to claim 3, which is provided in the Office Action. Despite the proper recitation of the applicable rule in

37 CFR 1.83(a) – that "the drawings must show every feature of the invention specified in the claims" – Applicants respectfully disagree with the assertion that the recitations "a control signal" and "the control signal" on lines 6 and 8 of claim 3 must be shown in the drawings or the features canceled from the claims. In this regard, Applicants respectfully assert that the "control signal" is not a feature of the invention.

The transistor circuit of claim 3 comprises a transistor device having a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal. The "control signal" is not a feature of the invention – the third terminal of the transistor device is the claimed feature. Accordingly, CFR 1.83(a) does not require Applicants to illustrate the "control signal" in the drawing or cancel the "control signal" from the claims. Nonetheless, in order to facilitate approval of the drawings, Applicants have amended the drawings to illustrate which terminal of the transistor device receives the control signal.

IV. Rejections Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 1 and 2 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Office Action states:

> Regarding claim 1, the recitation of "to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch" is indefinite because it is unclear how the third switch node can function as "an alternating (AC) ground". The third switch node, which is the control node of a transistor (gate or base), receives a signal (AC or DC) and it is not true that the third switch node will function as a ground. Claim 2 is indefinite because it depends on claim 1.

Applicants respectfully disagree with the assertion in the Office Action that the recitation of the language "to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch" in claim 1 is indefinite because, as the Examiner suggests, "it is unclear how the third switch node can function as an AC ground." Furthermore, Applicants respectfully disagree with the assertion in the Office Action that "it is not true that the third switch node will function as an [AC] ground."

As stated in the specification, it is known in the art that, in a high-frequency analog circuit, the control signal (*e.g.*, bias voltage, *etc.*) presented to a corresponding terminal in existing transistor-based switches is electrically an AC ground. *See, e.g.*, page 6, ll. 17 – 19; page 8, ll. 25 – 29. In this regard, with respect to the transistor circuit of claim 1, it should be appreciated that the circuit (*e.g.*, impedance circuit 708) connected to the third switch node (710) and the third terminal (712) of the transistor device (706) may be configured to "prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch."

Therefore, Applicants respectfully assert that the language "to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch" in independent claim 1 is not indefinite. Rather, this language clearly points out and distinctly claims the subject matter which Applicants regard as the invention. Accordingly, Applicants request that the Examiner reconsider and withdraw the rejection of independent claim 1 (and claim 2 which depends on claim 1) under 35 U.S.C. §112, second paragraph.

V. Claims 1 and 2 are Patentable Over U.S. Patent No. 4,678,947 to *Huijsing*

The Office Action rejects claim 1 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,678,947 to *Huijsing* ("the '947 patent"). Specifically, the Office Action

argues that figure 2 of the '947 patent shows all of the features of the transistor circuit of claim 1.

Applicants respectfully submit that independent claim 1 is allowable over the '947 patent for at least the reason that the '947 patent does not disclose, teach, or suggest that the circuit connected to the third switch node and the third terminal of the transistor device has "a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch and thereby reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device."

The Office Action argues that "A1 has very high input impedance." This argument, however, ignores all of the cited claimed feature by only focusing on the impedance of the circuit (A1, R1). Specifically, this argument ignores the fact that the '947 patent does not disclose, teach, or suggest the circuit connected to the third switch node and the third terminal of the transistor device having a "sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch and thereby reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device." In fact, the '947 does not disclose, teach, or suggest any relationship between the impedance of the circuit (A1, R1) and the function of the transistor device as a switch; nor does the '947 patent disclose, teach, or suggest any relationship between the impedance of the circuit (A1, R1) and the parasitic capacitance between the first terminal and the second terminal of the transistor device. Rather, the '947 patent discloses using the circuit (A1, R1) within the control system 8, to amplify an input voltage (V_{CS}) to produce a control voltage (V_C) for the transistor device. As stated in the Abstract, "[t]his downscales the forward voltage characteristics of the circuit from those of the transistor." Thus, the

circuit (A1, R1) disclosed in the '947 patent has nothing to do with the functioning of the transistor device as a switch and reducing the parasitic capacitance between the first terminal and the second terminal of the transistor device.

Accordingly, and for at least the reasons set forth above, independent claim 1 is believed to be allowable over the '947 patent. Furthermore, because claim 1 is believed to be allowable, dependent claim 2 (which depends on independent claim 1) should be allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

VI. Claims 3 – 5 are Patentable Over U.S. Patent No. 5,223,751 to *Simmons et al.*

The Office Action also rejects claims 3 – 5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,223, 751 to *Simmons et al.* ("the '751 patent"). Specifically, the Office Action argues that Figure 3 of the '751 patent discloses the transistor circuits of claims 3 – 5.

In the "Response to Arguments" on page 4, the Office Action responds to the arguments made in the "First Response and Amendment," in which Applicants asserted that the '751 patent does not disclose, teach, or suggest a transistor circuit for implementing a ***switch***, which comprises ***first and second switch nodes***.

Applicants respectfully assert that this rejection should be withdrawn because the '751 patent does not teach, disclose, or suggest all of the limitations of independent claim 3. Independent claim 3 is directed at a circuit for implementing a transistor-based ***switch***. Independent claim 3 contains the limitation of ***first and second switch nodes***. In addition, independent claim 3 contains the limitation of a transistor device having a terminal configured to receive a control signal for controlling the electrical connectivity between two

other terminals. Thus, independent claim 3 includes a transistor device and corresponding circuitry for implementing a ***switch***.

In contrast, the '751 patent does not disclose, teach, or suggest a transistor circuit for implementing a ***switch***, which comprises ***first and second switch nodes***. Furthermore, the '751 patent does not disclose, teach, or suggest the limitation of a transistor device having a terminal configured to receive a control signal for controlling the electrical connectivity between the other two terminals. In fact, the '751 patent does not make any reference to the use of a transistor circuit for implementing a switch. Rather, the '751 patent discloses a two-stage logic level shifter for reducing static current drain.

Furthermore, Applicants respectfully submit that independent claim 3 is allowable over the '751 patent for the additional reason that the '751 patent does not disclose, teach, or suggest that the circuit connected to the second terminal of the transistor device is configured "to provide a voltage to the second terminal when the control signal engages the transistor device to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit, thereby reducing noise injected to the external circuit at the first switch node." The '751 makes no mention of the transistor device implementing a switch. Furthermore, the '751 make no mention of configuring the circuit, which is connected to the second terminal of the transistor device, to improve the parasitic effects of the transistor device and thereby reduce noise injected to the external circuit at the first switch node. In fact, the '751 patent does not disclose, teach, or suggest any solution for improving the function of the transistor-based switch by reducing the parasitic effects of the transistor device.

Accordingly, and for at least these reasons, Applicants respectfully submit that independent claim 3 patently defines over the '751 patent and, therefore, is in condition for allowance. Furthermore, because independent claim 3 is believed to be allowable over the prior

art of record, dependent claim 4 (which depends from independent claim 3) and dependent claim 5 (which depends from independent claim 3) are allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 3 – 5 in condition for allowance.

VII. Claims 6 – 8 are Patentable Over U.S. Patent No. 4,752,703 to *Lin*.

After previously indicating that claims 6 – 8 would be allowable if rewritten to overcome the rejection under 35 U.S.C. §112, second paragraph, the Office Action now rejects claims 6 – 8 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,752,703 to *Lin* ("the '703 patent"). Specifically, the Office Action argues that the '703 patent discloses the transistor circuits of claims 6 – 8.

Applicants respectfully disagree with the characterization of the third transistor device (17) offered in the Office Action. The Office Action argues that the third transistor device (17) has a first terminal connected to the first terminal of the first transistor device (11), a second terminal connected to the second terminal of the second transistor device (12), and a third terminal configured to receive the control signal. As clearly illustrated in Figure 1 of the '703 patent, the second terminal of the third transistor (17) is not connected to the second terminal of the second transistor device (12). Clearly, the second terminal of the transistor device (17) is connected to a fourth transistor device (18) – not the second transistor device (12) as in independent claim 6. Therefore, Applicants respectfully submit that independent claim 6 is allowable over the '703 patent for at least the reason that the '703 patent does not disclose, teach, or suggest a "third transistor device having a first terminal connected to the first

terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal."

Furthermore, because independent claim 6 is believed to be allowable over the prior art of record, dependent claim 7 (which depends from independent claim 6) and dependent claim 7 (which depends from independent claim 6) are allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 6 – 8 in condition for allowance.

VIII. Claim 2 is Patentable Over U.S. Patent No. 4,678,947 to *Huijsing et al.*

The Office Action rejects claim 2 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,678,947 to *Huijsing et al.* ("the '947 patent"). The Office Action argues that the '947 patent discloses all of the limitations of claim 2 except for the limitation that the transistor device is a MOSFET transistor.

This rejection, however, is rendered moot because, as stated above, independent claim 1 is allowable over the '947 patent for at least the reason that the '947 patent does not disclose, teach, or suggest that the circuit connected to the third switch node and the third terminal of the transistor device has "a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch and thereby reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device." Furthermore, because independent claim 1 is believed to be allowable over the prior art of record, dependent claim 2 (which depends from independent claim 1) is allowable as a matter of law for at least the reason that it contains all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed.

Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claim 2 in condition for allowance.

CONCLUSION

In light of the foregoing remarks and for at least the reasons set forth above, Applicant respectfully submits that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1 - 8 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington D.C. 20231, on 7/30/02.

Stephanie Riley
Signature

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following claims have been amended by deleting the bracketed ("[]") portions and adding the underlined ("___") portions.

1. (amended twice) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a third switch node for receiving the control signal; and

a circuit connected to the third switch node and the third terminal of the transistor device, the circuit having a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch and thereby reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device.

2. (amended once) The transistor circuit of claim 1, wherein the transistor device is a metal-oxide-semiconductor field-effect transistor.

3. (amended once) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal; and

a circuit connected to the second terminal of the transistor device, the circuit configured to provide a voltage to the second terminal when the control signal engages the transistor device to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit, thereby reducing noise injected to the external circuit at the first switch node.

4. (amended once) The transistor circuit of claim 3, wherein the transistor device is a metal-oxide-semiconductor field-effect transistor.

5. (amended once) The transistor circuit of claim 3, wherein the circuit is an inverter circuit.